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GAZDZINSKI & ASSOCIATES
11440 WEST BERNARDO COURT, SUITE 375
SAN DIEGO, CA 92127

EXAMINER	
GARCIA OTERO, EDUARDO	

ART UNIT	PAPER NUMBER
2123	8

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,057	HANSSON, DANIEL	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2003 and 05 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6 and 7*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: Non-Final (first action on the merits)

Introduction

1. Title is: Method and Apparatus for Reducing Power Consumption in a Digital Processor.
2. First named inventor is: Hansson.
3. Claims 1-70 have been submitted, examined, and rejected. Claims 1, 21, 28, 36, 49, 55, 59, 64, 68, 69, and 70 are independent.
4. Priority is claimed to provisional US application filed on October 27, 2000.

Index of Important Prior Art

5. **Gupte** refers to US patent 5,996,083.
6. **Su** refers to "Low Power Architecture Design and Compilation Techniques for High-Performance Processors", by Ching-Long Su, et al., Abstract, Proceedings of COMPCON 1994, April 1994 (from Applicant's Information Disclosure Statement).
7. **Tabak** refers to "Advanced Microprocessors" by Danial Tabak, McGraw-Hill, Second Edition, 1995, ISBN 0-07-062843-2, chapter 5 Pipelining, pages 67-78.

Definitions

8. MS Dictionary refers to Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999:
   - **Flag** is defined at page 187, "n. 1. Broadly, a marker of some type used by a computer in processing or interpreting information; a signal indicating the existence or status of a particular condition...".
   - **Interrupt** is defined at page 246, "n. A signal from a device to a computer's processor requesting attention from the processor. When the processor receives an interrupt, it suspends its current operations, saves the status of its work, and transfers control to a special routine known as an interrupt handler... A hierarchy of interrupt priorities... A program can temporarily disable some interrupts if it needs the full attention of the processor to complete a particular task. *See also* exception, external interrupt, hardware interrupt, internal interrupt, software interrupt."

35 USC § 112- first paragraph- enablement

9. The following is a quotation of the first paragraph of 35 U.S.C. 112: The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such

full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. **Claims 6 is rejected under 35 U.S.C. 112, first paragraph,** as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

11. The claim 6 term **"preventing the setting of interrupt flags from that point when the interrupt flags are cleared until said pipeline is stalled"** is not enabled. Claim 6 depends from claim 2, which depends from claim 1. There has been no antecedent discussion or definition of precisely when (at what point) said interrupt flags are cleared. Specifically, claim 1 stalls and eventually restarts the pipeline without any discussion of clearing or setting interrupt flags.

12. Note MS Dictionary page 246 states "A program can temporarily disable some interrupts if it needs the full attention of the processor to complete a particular task". Additionally, claim 1 stalls the pipeline until "a predetermined event" such as the claim 2 "interrupt". The timing of events appears important..

35 USC § 112-Second Paragraph-indefinite claims

13. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. **Claims 4, 6, 7, 11, 21, and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15. The claim 4 term **"said predetermined event comprises a restart condition, said processor being re-enabled after having been halted"** is indefinite. Note that ancestor independent claim 1 "stall"s the pipeline, and "disable"s the memory. Claim 1 uses the term "disable" with respect to memory, not with respect to "processor". Similarly, claim 1 does not use the term "halt". Using exact and consistent terminology is critical. For example, Power PC has four different and mutually exclusive states: Full On, Doze, Nap, and Sleep

(see Gupte column 2). Disabling memory may be different than disabling processor, and "halt" may be different than "stall", and restarting pipeline may be different than restarting processor.

16. The claim 6 term **"preventing the setting of interrupt flags from that point when the interrupt flags are cleared until said pipeline is stalled"** is indefinite. Claim 6 depends from claim 2, which depends from claim 1. There has been no antecedent discussion or definition of precisely when (at what point) said interrupt flags are cleared. Specifically, claim 1 stalls and eventually restarts the pipeline without any discussion of clearing or setting interrupt flags.
17. Additionally, MS Dictionary does not have a definition for the term "interrupt flags".
18. Note specification page 14 line 14 states "sets the interrupt flags in the main memory, the latter required to be cleared before entering the sleep mode" and page 14 line 19 "the interrupt enable flags are disabled so that no new interrupt requests...". Thus, claim 6 appears related to specification page 14, but is not clear. Apparently the intent is to: save the current interrupt flag settings, then disable any new interrupts, then process the saved current interrupts, then sleep. Please clarify the precise events and timing of claim 6 in relation to antecedent claim 2 and antecedent claim 1.
19. The claim 7 term **"providing a flag setting branch instruction"** is indefinite. Branching instructions appear distinct from flag setting instructions. See FIG 1b.
20. Also in claim 7, [2]-**"disposing said first instruction in said delay slot of said flag setting branch instruction" is indefinite.** Note "delay slot" is defined as "the slot within a pipeline subsequent to a branching or jump instruction being decoded" at specification page 13. It is not clear what is intended by the term "disposing" said first instruction in said delay slot. Note that claim 1 already states: "defining" and "providing" and "decoding" and "executing" said first instruction
21. Further, specification page 15 line 3 states "disposing the SLEEP instruction in a delay slot of a flag setting jump that restores the interrupt enable flags". The term "disposing" appears to similar or equivalent to the term "providing" in claim 1. Further, it is not clear which instruction is restoring the interrupt enable flags: the SLEEP instruction or the jump instruction.

22. Additionally, it is not clear what flags are referred to in claim 7: the "interrupt enable flags" of specification page 15 line 3, or the "SLEEP mode flag (ZZ) of specification page 11 line 6, or some other flags.
23. The claim 11 term **"first and second enable signals"** is indefinite. It is not clear whether how said first and second enable signals differ, if they differ at all. It is not clear whether said signals are flags.
24. Also in claim 11, the term **"valid data"** is indefinite. It is not clear whether "valid data" is the opposite of "data will not be used in a later stage of said pipeline" from antecedent claim 10.
25. The claim 21 term **"detecting, using said logic circuit, that the predetermined condition exists with respect to certain of said data"** is indefinite. Specifically, it is not clear what is intended by the term "predetermined condition".
26. The claim 28 term **"validity"** is indefinite. The apparently related term "valid data" is stated at specification page 21 line 4, but is not adequately defined.

Claim Interpretation

27. **The claim language is interpreted in light of the specification.** Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns,* 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).
28. The claim 2 term **"program interrupt"** is interpreted as "interrupt". Note that MS Computer Dictionary has does not have a definition for "program interrupt", but does have definitions for: interrupt, exception, external interrupt, hardware interrupt, internal interrupt, and software interrupt.
29. The claim 7 term **"delay slot"** is defined as "the slot within a pipeline subsequent to a branching or jump instruction being decoded" at specification page 13.

35 USC § 102: filed before 11/29/00 and not vol. pub. under 35 USD 122(b)

30. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another

who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

31. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

32. Claims 1-18, 20-34, and 36-70 are rejected under 35 U.S.C. 102(e).

33. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Gupte.

34. Independent claim 1 is "method of operating a pipelined digital processor having a memory" claim with 7 limitations, numbered by the Examiner for clarity.

35. [1]-**"defining a first instruction, said first instruction being adapted to stall the pipeline of said processor upon execution thereof"** is disclosed by Gupte column 3 line 41-63 "A microprocessor is provided which includes improved power management facilities. The microprocessor includes a power control register that includes a plurality of fields for individually controlling the power consumption of the individual functional units within the microprocessor. The power control register fields can be set by software which has the much greater ability to look out into the future to determine whether the functional units will be required. This allows the microprocessor to shut down or adjust the execution rate of any one of the functional units when the software determines that the functional unit is not required by the currently executing software. This offloads the task of dynamically sensing and decoding instruction activity from the hardware to the software. In addition, software control permits power management capabilities not possible with hardware. For example, software can disable branch prediction hardware during execution of a certain block of code in order to save power. The software can also slow or shut down an external bus interface to main memory in the event a certain block of code is expected to fit entirely within an internal cache. Software possesses knowledge that is unavailable to hardware and can thus make more informed power management decisions that have the least impact on performance." and column 4 line 45 "stall signal" and column 13 line 1 "stalling the pipeline" and FIG 10

"STALL LOGIC. Note that Gupte's term "set by software software" implies providing, defining, providing, decoding, and executing instructions.

36. [2]-**"providing said first instruction within said pipeline"** is disclosed by Gupte column 3 line 45 "power control register fields can be set by software" and column 13 line 1 "stalling the pipeline". Note that Gupte's term "software" implies providing, defining, providing, decoding, and executing instructions.
37. [3]-**"decoding said first instruction"** is disclosed by Gupte column 3 line 45 "power control register fields can be set by software" and column 13 line 1 "stalling the pipeline".
38. [4]-**"executing said first instruction"** is disclosed by Gupte column 3 line 45 "power control register fields can be set by software" and column 13 line 1 "stalling the pipeline".
39. [5]-**"stalling said pipeline in response to said first instruction"** is disclosed by Gupte column 3 line 45 "power control register fields can be set by software" and column 13 line 1 "stalling the pipeline".
40. [6]-**"disabling said memory in response to said first instruction"** is disclosed by Gupte column 2 line 62 "disabling the memory" and column 3 line 48 "shut down or adjust the execution rate of any one of the functional units" and column 4 line 12 "random access memory (RAM)" and column 5 line 54 "multiported cache memory unit".
41. [7]-**"restarting said pipeline and enabling said memory upon the occurrence of a predetermined event"** is disclosed by Gupte column 4 line 30 "wake up".
42. Claims 2- are rejected under 35 U.S.C. 103(a) as being unpatentable over
43. Claims 2- depend directly or indirectly from claim 1.
44. In claim 2, **"said predetermined event comprises a program interrupt"** is disclosed by Gupte column 2 line 5 "interrupt service routine".
45. In claim 3, **"said program interrupt comprises transfer of programmatic control to an interrupt service routine"** is disclosed by Gupte column 2 line 5 "interrupt service routine".
46. In claim 4, **"said predetermined event comprises a restart condition, said processor being re-enabled after having been halted"** is disclosed by Gupte column 1 line 67 to column 2 line 4 "microprocessor activates or "wakes up" the subsystem... interrupt service routine".

47. In claim 5, **"waiting for a wait state duration time after said act of disabling but before said pipeline is restarted"** is disclosed by Gupte column 4 line 28 "power latency value (PLV) in units of clock cycles" and column 4 line 30 "wake up".
48. In claim 6, **"preventing the setting of interrupt flags from that point when the interrupt flags are cleared until said pipeline is stalled"** is disclosed by Gupte column 2 line 4 "interrupt service routing (sic) which is invoked by a non-maskable interrupt". Note that interrupts are generally hierarchical (some have higher priority).
49. In claim 7, there are two limitations:
50. [1]-**"providing a flag setting branch instruction having a delay slot within said pipeline"** is disclosed by Gupte column 3 line 55 "branch" and column 2 line 5 "interrupt service routine".
51. [2]-**"disposing said first instruction in said delay slot of said flag setting branch instruction"** is disclosed by Gupte column 3 line 55 "branch" and column 2 line 5 "interrupt service routine".
52. Regarding claim 7. Further, note that "delay slot" is defined as "the slot within a pipeline subsequent to a branching or jump instruction being decoded" at specification page 13.
53. Additionally, Gupte broadly discloses column 3 line 45 "power control register fields can be set by software" and column 13 line 1 "stalling the pipeline" and column 2 line 5 "interrupt service routine". It does not appear that placing the claim 1 "stalling" and "disabling" instruction in the delay slot (immediately after a branching instruction) has any novel or unexpected results. *In re Japikse*, 181 F.2d 1019, 86 USPQ 70, 73 (CCPA 1950) states "no invention in shifting the starting switch disclosed by Cannon to a different position since the operation of the device would not thereby be modified", and *In re Kuhle,* 526 F.2d 553, 188 USPQ 7 (CCPA 1975) states "the particular placement provided no novel or unexpected result". See also MPEP § 2144.04(VI)(C).
54. In this claim, placing the instruction in the delay slot does not provide novel results, and does not provide unexpected results. The discussion at specification page 13 and 14 regarding the program counter (PC) appears to be ordinary bookkeeping associated with interrupts and with branching. Also, the discussion at specification page 14 regarding disabling the interrupt flags appears to be ordinary interrupt routine procedures. Note MS Dictionary

defines "interrupt" as "A signal from a device to a computer's processor requesting attention from the processor. When the processor receives an interrupt, it suspends its current operations, saves the status of its work, and transfers control to a special routine known as an interrupt handler... A hierarchy of interrupt priorities... A program can temporarily disable some interrupts if it needs the full attention of the processor to complete a particular task. *See also* exception, external interrupt, hardware interrupt, internal interrupt, software interrupt." Thus, one of ordinary skill in the art would interpret Gupte as disclosing the ordinary bookkeeping associated with interrupts and with branching.

55. In claim 8, there are 5 limitations:
56. [1]-**"providing a logic circuit adapted for detection of a predetermined condition of the data within the pipeline"** is disclosed by Gupte FIG 10 "STALL LOGIC".
57. [2]-**"inserting data into the pipeline"** is disclosed by Gupte FIG 10 "PIPELINE CONTROL UNIT".
58. [3]-**"detecting, using said logic circuit, that the predetermined condition exists with respect to certain of the data"** is disclosed by Gupte FIG 10 "STALL LOGIC".
59. [4]-**"invoking a sleep mode within the pipeline in response to said detected condition if no such sleep mode is already invoked"** is disclosed by Gupte FIG 10 "STALL LOGIC".
60. [5]-**"and permissively restarting the pipeline when the condition no longer exists"** is disclosed by Gupte FIG 10 "STALL LOGIC".
61. In claim 9, **"said act of permissively restarting said pipeline comprises restarting said pipeline only if restart has been or is concurrently enabled by the occurrence of said predetermined event"** is disclosed by Gupte column 4 line 43 "If the unit is going to take longer than PLV number of cycles to become available, it asserts a stall signal to stall further execution until it does become available".
62. In claim 10, "said act of detecting said predetermined condition of said data comprises using said logic circuit to detect when said data will not be used in a later stage of said pipeline" is disclosed by Gupte column 3 line 46 "look out into the future".
63. In claim 11, **"said act of detecting when said data will not be used comprises detecting the activation, of first and second enable signals, said first and second enable signals**

being activated if the current pipeline stage contains valid data" is disclosed by Gupte column 3 line 46 "look out into the future".

64. In claim 12, **"providing a plurality of extension instructions within the instruction set architecture of said processor; wherein said act of activating said second enable signal comprises enabling the data path to the arithmetic logic unit (ALU) with respect to all of said plurality of extension instructions"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
65. In claim 13, **"said act of detecting said predetermined condition comprises detecting the anticipatory execution of an instruction within said pipeline, said instruction being subsequently stopped by a conditional evaluation conducted by said processor"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
66. In claim 14, **"said act of detecting said predetermined condition comprises detecting the anticipatory execution of an instruction within said pipeline, said instruction being subsequently stopped by a conditional evaluation"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
67. In claim 15, **"switching off a plurality of clocks within said processor in response to said act of stalling"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
68. In claim 16, **"preserving the clocks serving the interface module and timer of said processor in an active state"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
69. In claim 17, **"changing the status of at least one debug flag, said act of changing status thereby disabling at least one debug clock associated with said processor"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
70. In claim 18, **"limiting the number of nodes within at least a portion of the gate logic of said processor that toggle per clock cycle"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
71. In claim 19, see 35 USC 103 below.

72. In claim 20, **"limiting the number of nodes within at least a portion of the gate logic of said processor that toggle per clock cycle"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
73. In claim 21, there are 5 limitations:
74. [1]-**"inserting a plurality of data into said pipeline"** is disclosed by Gupte FIG 10 "PIPELILNE CONTROL UNIT".
75. [2]-**"detecting, using said logic circuit, that the predetermined condition exists with respect to certain of said data"** is disclosed by Gupte FIG 10 "PIPELINE CONTROL UNIT".
76. [3]-**"stalling said pipeline in response to said detected condition if no such pipeline stall is already invoked"** disclosed by Gupte FIG 10 "STALL LOGIC".
77. [4]-**"checking for the presence of said condition at least once thereafter"** is disclosed by Gupte FIG 10 "STALL LOGIC," and column 4 line 28 "power latency value (PLV) in units of clock cycles", and column 4 line 30 "wake up".
78. [5]-**"restarting the pipeline when said detected condition no longer exists"** is disclosed by Gupte FIG 10 "PIPELINE CONTROL UNIT", and column 4 line 30 "wake up".
79. In claim 22, **"said act of restarting said pipeline comprises permissively restarting said pipeline only if restart has been or is concurrently enabled by the occurrence of a predetermined event"** is disclosed by Gupte column 2 line 4 "interrupt service routing (sic) which is invoked by a non-maskable interrupt".
80. In clam 23, **"said predetermined event comprises a program interrupt request (IRQ)"** is disclosed by Gupte column 2 line 4 "interrupt service routing (sic) which is invoked by a non-maskable interrupt".
81. In claim 24, **"said act of detecting said predetermined condition of said data comprises using said logic circuit to detect when said data will not be used in a later stage of said pipeline"** is disclosed by Gupte column 3 line 46 "look out into the future".
82. In claim 25, **"said act of detecting when said data will not be used comprises detecting the activation of first and second enable signals, said first and second enable signals being activated if the current pipeline stage contains valid data"** is disclosed by Gupte column 3 line 46 "look out into the future".

83. In claim 25, **"said act of activating said second enable signal comprises enabling the data path to the arithmetic logic unit (ALU) with respect to all extension instructions of said processor"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
84. In claim 27, **"said act of detecting said predetermined condition comprises detecting the anticipatory execution of an instruction within said pipeline, said instruction being subsequently stopped by a conditional evaluation conducted by said processor"** is disclosed by Gupte column 3 line 46 "look out into the future ", and column 2 line 4 "interrupt service routing (sic) which is invoked by a non-maskable interrupt".
85. In claim 28, there are 3 limitations:
86. [1]-**"a pipeline having at least fetch, decode, and execute stages, said pipeline adapted to process a plurality of instructions and data therein, said pipeline further being adapted to allow for stalling thereof, said plurality of instructions comprising at least one extension instruction"** is disclosed by Gupte FIG 10 "PIPELINE CONTROL UNIT" and "STALL LOGIC".
87. [2]-**"an arithmetic logic unit (ALU) operatively coupled to said pipeline, said ALU processing at least a portion of said data based at least in part on said at least one extension instruction"** is disclosed by Gupte FIG 10 "PIPELINE CONTROL UNIT" and "STALL LOGIC" and FIG 1 "CPU".
88. [3]-**"detect the validity of at least one portion of said data present in a first stage of said pipeline... initiate a stall condition in said pipeline... re-evaluate the validity of said data after said stall condition is initiated... remove said stall condition when said at least portion of said data is valid"** is disclosed by Gupte FIG 10 "PIPELINE CONTROL UNIT" and "STALL LOGIC" and column 3 line 46 "look out into the future".
89. In claim 29, "first and second enable signal logic generating respective first and second enable signals when said first pipeline stage contains valid data" is disclosed by Gupte FIG 10 "PIPELINE CONTROL UNIT" and "STALL LOGIC" and column 3 line 46 "look out into the future".

90. In claim 30, **"said second enable signal enables at least a portion of the data path to said ALU"** is disclosed by Gupte FIG 10 "PIPELINE CONTROL UNIT" and "STALL LOGIC" and column 3 line 46 "look out into the future".
91. In claim 31, **"said logic is further adapted to detect the anticipatory execution of a first instruction within said pipeline, said first instruction being subsequently stopped by a conditional evaluation conducted by said processor"** is disclosed by Gupte FIG 10 "PIPELINE CONTROL UNIT" and "STALL LOGIC" and column 3 line 46 "look out into the future".
92. In claim 32, **"further comprising a plurality of clocks, wherein said processor is further adapted to switch off at least a portion of said plurality of clocks in response to said stall condition"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
93. In claim 33, **"said plurality of clocks excludes the clocks serving the interface module and timer of said processor"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
94. In claim 34, **"at least one debug clock... at least one debug flag...logic adapted to change the status of said at least one debug flag, said status change disabling said at least one debug clock"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units".
95. In claim 35, see 35 USC 103 rejection below.
96. In claim 36, **"a processor core having a pipeline with at least fetch, decode, and execute stages, said pipeline adapted to process a plurality of instructions and data therein, including at least one first instruction adapted to stall said pipeline; an arithmetic logic unit (ALU) operatively coupled to said pipeline, said ALU being adapted to process at least a portion of said data based on said instructions; first logic operatively coupled to said pipeline and adapted to detect the presence of said at least one first instruction within said pipeline and stall said pipeline upon execution thereof; second logic operatively coupled to said pipeline and adapted to restart said pipeline after stalling upon the occurrence of a predetermined event"** is disclosed by Gupte FIG 10 "PIPELINE

CONTROL UNIT" and "STALL LOGIC" and column 3 line 46 "look out into the future" and FIG 1 CPU.

97. In claim 37, **"a data storage device operatively coupled to said processor core: and third logic operatively coupled to said first logic and said data storage device, said third logic being configured to disable said data storage device upon the stalling of said pipeline by said first logic"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units" and FIG 1 "MAIN MEMORY" and "DISK".

98. In claim 38, **"fourth logic adapted to re-enable said data storage device upon restart of said pipeline by said second logic"** is disclosed by Gupte column 3 line 48 "shut down or adjust the execution rate of any of the functional units" and FIG 1 "MAIN MEMORY" and "DISK".

99. In claim 39, **"detect the validity of at least a portion of said data present in said pipeline... initiate a stall condition in said pipeline if said at least portion is not valid... re-evaluate the validity of said data at least once after said stall condition is initiated... remove said stall condition when said at least portion of said data is valid"** is disclosed by Gupte FIG 10 "PIPELINE CONTROL UNIT" and "STALL LOGIC" and column 3 line 46 "look out into the future"

100. In claim 40, **"first and second enable signal logic, said first and second enable signal logic generating respective first and second enable signals when said pipeline contains valid data"** is disclosed by Gupte FIG 10 "PIPELINE CONTROL UNIT" and "STALL LOGIC" and column 3 line 46 "look out into the future"

101. In claims 41-70, all limitations are disclosed by Gupte FIG 1 "CPU" and "MAIN MEMORY" and "DISK", and FIG 2 "POWER CONTROL" and "LATENCY CONTROL", FIG 3 "CLOCK GENERATOR" and "CLOCK DIVIDER", FIG 5 "ENABLE", FIG 7 "STALL LOGIC" and "PIPELINE CONTROL UNIT", FIG 11 "DOWN COUNTER" and "CHANGE DETECTOR", column 1 line 67 "wakes up", column 2 line 5 "interrupt service routine" and line 62 "disabling the memory", column 3 line 7 "check the queued instructions" and line 46 "look out into the future" and line 48 "shut down or adjust" and line 55 "disable branch", column 4 line 11 "functional unit is a multiported random access memory" and line 45 "stall signal", and column 5 line 55 "branch prediction unit".

Claim Rejections - 35 USC § 103

102. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

103. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: Determining the scope and contents of the prior art. Ascertaining the differences between the prior art and the claims at issue. Resolving the level of ordinary skill in the pertinent art. Considering objective evidence present in the application indicating obviousness or nonobviousness.

104. Claims 19 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable.

105. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gupte in view of Su.

106. Claim 19 depends from claim 18 with one additional limitation.

107. Gupte does not disclose the additional limitation.

108. **"limiting the number of bits in a binary sequence present within said data that change per clock cycle to a predetermined number"** is disclosed by Su Abstract "Reducing switching activity would significantly reduce power consumption... Grey code addressing... only one-bit different".

109. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Su to modify Gupte. One of ordinary skill in the art would have been motivated to do this in order to save switching related power using Gupte to shut down entire functional units, and then to save additional switching power by using Su's Gray codes which have only a singe bit difference between consecutive numbers. Note that Gupte and Su power saving techniques are independent of each other, and thus can be used simultaneously without any interference.

110. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gupte in view of Su.

111. Claim 35 depends from claim 28 with one additional limitation.

112. Gupte does not disclose the additional limitation.

113. **"said logic is further configured to limit the number of bits present in a binary sequence that change per clock cycle to a predetermined number"** is disclosed by Su Abstract "Reducing switching activity would significantly reduce power consumption... Grey code addressing... only one-bit different".

114. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Su to modify Gupte. One of ordinary skill in the art would have been motivated to do this in order to save switching related power using Gupte to shut down entire functional units, and then to save additional switching power by using Su's Gray codes which have only a singe bit difference between consecutive numbers. Note that Gupte and Su power saving techniques are independent of each other, and thus can be used simultaneously without any interference.

Additional Cited Prior Art

115. The following US patents or publications are hereby cited as prior art, but have not been used for rejection. Applicant should review these carefully before responding to this office action.

116. "Advanced Microprocessors" by Danial Tabak, McGraw-Hill, Second Edition, 1995, ISBN 0-07-062843-2, chapter 5 Pipelining, pages 67-78.

117. US patent 6,438,700 discloses conditionally turning off coprocessor clock at Abstract.

118. US patent 6,347,397 discloses turning off clocks and supplying low voltage at Abstract.

Conclusion

119. All pending claims stand rejected.

Communication

120. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Tuesday through Friday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's

supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * *

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER